07-14-00

Attorney Docket No. SEL 194

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION TRANSMITTAL LETTER

Transmitted herewith for filing is the patent application of:

1. Inventor(s): Hideomi SUZAWA and Koji ONO

2. Title: Wiring And Manufacturing Method Thereof, Semiconductor Device Comprising Said Wiring, And Dry Etching Method

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Enclosed are:

X	18	Sheets of Drawings
		Formal
	X	Informal
X		Assignment of invention to Semiconductor Energy Laboratory Co., Ltd.
X	29	Pages of Specification
X	6	Pages of Claims
X		Abstract of The Disclosure
		Statement of Small Entity
X		Declaration and Power of Attorney

X Information Disclosure Statement

X Appointment of Associate Attorneys

Applicants claim priority under 35 USC §119 to the following foreign application:

Serial no. 11-206954 filed July 22, 1999 in Japan.

X A certified copy of this priority document is enclosed herewith.

Please enter the enclosed preliminary amendment prior to calculation of the fees.

Claims as Filed

	Number Filed		Number Extra	Rate	Fee
Total	40	-20	20	(small entity) x 9 (others) x 18	$360.00
Independent	11	-3	8	(small entity) x 39 (others) x 78	$624.00
Multiple Dependent	No			(small entity) x 130 (others) x 260	$0.00
Basic Fee				(small entity) x 345 (others) x 690	$690.00
Assignment					$40.00
Total Fee					$1714.00

_____ Please charge my Deposit Account No. 50/1039 in the amount of $ _____. A duplicate copy of this sheet is enclosed.

X The Commissioner is hereby authorized to charge any additional fees (except the issue fee) which may be required at any time during the prosecution of this application without specific authorization, or credit any overpayment to Deposit Account No. 50/1039. A duplicate copy of this sheet is enclosed.

X A check in the amount of $1714 is enclosed to cover the filing fee and the recordation of the Assignment, if any, transmitted herewith.

Date: July 5, 2000

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Name Tricia Senese
(typed or printed)

Signature Tricia Senese

Attorney Docket no: SEL 194

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
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Suzawa et al.)
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Serial No.:)
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For: Wiring And Manufacturing Method Thereof,) Semiconductor Device Comprising Said) Wiring, And Dry Etching Method)
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Examiner:)
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Art Unit:)

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July 5, 2000

Assistant Commissioner for Patents
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PRELIMINARY AMENDMENT A

Prior to calculation of fees and examination, please enter the following amendment in the above-identified application:

IN THE CLAIMS:

Please amend the claims as follows:

Claim 3, ln. 1, delete "or 2".

Claim 4, ln. 1, delete "or 2".

Claim 8, ln. 1, delete "or 7".

Claim 9, ln. 1, delete "or 7".

Claim 10, ln. 1, delete "or 7".

Claim 11, ln. 1, delete "or 7".

Claim 18, ln. 1, delete "or 17".

Claim 19, ln. 1, delete "or 17".

Claim 27, ln. 1, delete "or 26".

Please add the following new claims:

-- 32. The wiring according to claim 2, wherein said metallic alloy film is an alloy film of one element, or a plurality of elements, selected from the group consisting of Ta; Ti; Mo; Cr; Nb; and Si, and tungsten. --

-- 33. The wiring according to claim 2, wherein said metallic compound film is a nitride film of tungsten.--

-- 34. The semiconductor device according to claim 7, wherein said wiring is a gate wiring of a thin film transistor.--

-- 35. The semiconductor device according to claim 7, wherein said semiconductor device is an active matrix type liquid crystal display device. --

-- 36. The semiconductor device according to claim 7, wherein said semiconductor device is an EL display device.--

-- 37. The semiconductor device according to claim 7, wherein said semiconductor device is one selected from the group consisting of a video camera, a digital camera, a projector, a goggle type display, a car navigation system, a personal computer, or a portable information terminal. --

-- 38. The method of forming a wiring according to claim 17, wherein said etching is performed using an etching gas comprising a mixed gas of a first reaction gas containing fluorine and a second reaction gas containing chlorine, and a specific selectivity in said etching gas between said base film and said metallic thin film is 2.5 or more. --

-- 39. The method of forming a wiring according to claim 17, wherein said metallic thin film is a thin film, or a laminated film of thin films, selected from the group consisting of: tungsten film; a metallic compound film having a tungsten compound film as its main constituent; and a metallic alloy film having a tungsten alloy as its main constituent. --

-- 40. The method of dry etching according to claim 26, wherein said method of dry etching uses an ICP etching device. --

REMARKS

This amendment is being submitted to remove multiple dependencies in the claims. It is believed that no new matter is being added. Accordingly, it is requested that this amendment be entered.

Respectfully submitted,

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WIRING AND MANUFACTURING METHOD THEREOF, SEMICONDUCTOR DEVICE COMPRISING SAID WIRING, AND DRY ETCHING METHOD

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device having a circuit comprised of a thin film transistor (hereafter referred to as TFT), and a method of manufacturing thereof. For example, the present invention relates to an electro-optical device typified by a liquid crystal display panel, and to electronic equipment in which the electro-optical device is installed as a part. In particular, the present invention relates to a dry etching method of etching a metallic thin film, and to a semiconductor device provided with a tapered shape wiring obtained by the dry etching method.

Note that throughout this specification, the term semiconductor device denotes a general device which functions by utilizing semiconductor characteristics, and that electro-optical devices, semiconductor circuits, and electronic equipments are all semiconductor devices.

2. Description of the Related Art

Techniques of structuring a thin film transistor (TFT) using a semiconductor thin film (having a thickness on the order of several nm to several hundred of nm) formed on a substrate having an insulating surface have been in the spotlight in recent years. Thin film transistors are widely applied to electronic devices such as an IC and an electro-optic device, and in particular, development of the TFT as a switching element of a pixel display device is proceeding rapidly.

Conventionally, Al is often used in a TFT wiring material due to things such as its ease of workability, its electrical resistivity, and its chemical resistance. However, when using Al in a TFT wiring, the formation of a protuberance such as a hillock or a whisker due to

heat treatment, and the diffusion of aluminum atoms into a channel forming region, causes poor TFT operation and a reduction of TFT characteristics. High heat resistance tungsten (W), with a relatively low bulk resistivity of 5.5 $\mu\Omega$·cm, can therefore be given as a preferable wiring material other than Al as a wiring material.

Further, in recent years, the demands of micro-processing techniques have become severe. In particular, with changes in high definition and large screens of a liquid crystal display, high selectivity in the wiring processing step as well as extremely strict control of line width is required.

A general wiring process can be performed by wet etching using a solution or by dry etching using a gas. However, when considering miniaturization of the wiring, maintenance of repeatability, reduction of waste, and decrease of cost, wet etching is unfavorable, and therefore dry etching is considered favorable for wiring processing.

When processing tungsten (W) by dry etching, a mixed gas of SF_6 and Cl_2 is generally used as an etching gas. While micro-processing with a large etching rate in a short time is possible when this gas mixture is used, it is difficult to obtain a desirable tapered shape. In order to improve the coverage of a lamination film formed on the wiring, there are cases in which the cross section of the wiring is made an intentional forward taper, depending upon the device structure.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a method of dry etching for patterning an etching layer made from tungsten (W) or a tungsten compound so as to give the cross section a forward tapered shape. Further, another object of the present invention is to provide a method of controlling the dry etching method so as to have a uniform, arbitrary taper angle over the entire etching layer, with no dependence upon location. In addition, another object of the present invention is to provide a semiconductor device using a wiring having the arbitrary taper angle obtained from the above method, and a method of

manufacturing the semiconductor device.

A structure of the present invention disclosed in this specification relating to a wiring is:

a wiring having a tungsten film, a metallic compound film having a tungsten compound as its main constituent, or a metallic alloy film having a tungsten alloy as its main constituent, characterized in that a taper angle α is within a range of 5° to 85°.

Further, another structure of the present invention relating to a wiring is:

a wiring having a lamination structure of laminated thin films selected from the group consisting of: a tungsten film; a metallic compound film having a tungsten compound as its main constituent; and a metallic alloy film having a tungsten alloy as its main constituent, characterized in that a taper angle α is within a range of 5° to 85°.

In each of the above structures, the metallic alloy film is characterized in that it is an alloy film of one element, or a plurality of elements, selected from the group consisting of: Ta; Ti; Mo; Cr; Nb; and Si, and tungsten.

Furthermore, the metallic compound film is characterized in that it is a nitride film of tungsten in each of the above structures.

Moreover, in order to increase adhesion in each of the above structures, a silicon film having conductivity (for example, a phosphorous doped silicon film or a boron doped silicon film) may be formed as the lowest layer of the wiring.

A structure of the present invention relating to a semiconductor device is:

a semiconductor device provided with a wiring made from a tungsten film, a metallic compound film having a tungsten compound as its main constituent, or a metallic alloy film having a tungsten alloy as its main constituent, in which a taper angle α is within a range of 5° to 85°.

Further, another structure of the present invention relating to a semiconductor device is:

a semiconductor device provided with a wiring made from a lamination structure of

laminated thin films selected from the group consisting of: a tungsten film; a metallic compound film having a tungsten compound as its main constituent; and a metallic alloy film having a tungsten alloy as its main constituent, in which a taper angle α is within a range of 5° to 85°.

In each of the above semiconductor related structures, the wiring is characterized in that it is a gate wiring of a TFT.

Furthermore, a structure of the present invention relating to a method of manufacturing a wiring is:

a method of manufacturing a wiring, comprising:

a step of forming a metallic thin film on a base film;

a step of forming a resist pattern on the metallic thin film; and

a step of forming the wiring, in which a taper angle α is controlled in accordance with bias power density, by performing etching of the metallic thin film having the resist pattern.

Moreover, another structure of the present invention relating to a method of manufacturing a wiring is:

a method of manufacturing a wiring, comprising:

a step of forming a metallic thin film on a base film;

a step of forming a resist pattern on the metallic thin film; and

a step of forming the wiring, in which a taper angle is controlled in accordance with flow rate of a gas containing fluorine, by performing etching of the metallic thin film having the resist pattern.

In each of the above structures relating to methods of manufacturing a wiring:

the method of manufacturing is characterized in that:

the etching is performed using an etching gas comprised of a mixed gas of a first reaction gas containing fluorine and a second reaction gas containing chlorine; and

the specific selectivity in the etching gas between the base film and the metallic

thin film is greater than 2.5.

Further, the metallic thin film in each of the above structures relating to methods of manufacturing a wiring is characterized in that it is a thin film, or a lamination film of thin films, selected from the group consisting of: a tungsten film; a metallic compound film having a tungsten compound film as its main constituent; and a metallic alloy film having a tungsten alloy as its main constituent.

A structure of the present invention relating to a method of dry etching is:

a method of dry etching having the removal by an etching gas of a desired portion of a thin film selected from the group consisting of: a tungsten film; a metallic compound film having a tungsten compound film as its main constituent; and a metallic alloy film having a tungsten alloy as its main constituent, characterized in that the etching gas is a mixed gas of a first reaction gas containing fluorine and a second reaction gas containing chlorine.

In the above structure of the present invention relating to the dry etching method, the first reaction gas is characterized in that it is a gas selected from the group consisting of CF_4, C_2F_6, and C_4F_8.

Further, in the above structure of the present invention relating to the dry etching method, the second reaction gas is characterized in that it is a gas selected from the group consisting of Cl_2, $SiCl_4$, and BCl_3.

Moreover, the etching method is characterized in that it uses an ICP etching device in the above structure of the present invention related to a method of dry etching.

The above structure of the present invention relating to the dry etching method is further characterized in that a taper angle α is controlled in accordance with the bias power density of the ICP etching device.

Another structure of the present invention relating to a method of dry etching is:

a method of dry etching characterized in that a taper angle of an inside sidewall of a formed hole or recess is controlled in accordance with bias power density.

In addition, another structure of the present invention relating to a method of dry

etching is:

a method of dry etching characterized in that a taper angle of an inside sidewall of a formed hole or recess is controlled in accordance with specific gas flow rate.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

Fig. 1 is a diagram showing the dependence of a taper angle α on bias power;

Fig. 2 is a diagram showing the dependence of the taper angle α on specific CF_4 flow rate;

Fig. 3 is a diagram showing the dependence of the taper angle α on specific (W / resist) selectivity;

Fig. 4 is a drawing showing a plasma generation mechanism of an ICP etching device;

Fig. 5 is a diagram showing a multi-spiral coil method ICP etching device;

Figs. 6A and 6B are explanatory diagrams for a taper angle α;

Figs. 7A to 7C are cross sectional SEM photographs of wirings;

Figs. 8A and 8B are cross sectional SEM photographs of wirings;

Figs. 9A and 9B are diagrams showing the dependence of etching rate and specific (W / resist) selectivity on bias power;

Figs. 10A and 10B are diagrams showing the dependence of etching rate and specific (W / resist) selectivity on specific CF_4 flow rate;

Figs. 11A and 11B are diagrams showing the dependence of etching rate and specific (W / resist) selectivity on ICP power;

Fig. 12 is a cross sectional diagram of an active matrix type liquid crystal display device;

Fig. 13 is a cross sectional diagram of an active matrix type liquid crystal display device;

Fig. 14 is a cross sectional diagram of an active matrix type liquid crystal display device;

Figs. 15A to 15F are cross sectional diagrams of wirings;

Fig. 16 is a diagram showing the structure of an active matrix type EL display device;

Fig. 17 is a diagram showing a perspective view of an AM-LCD;

Figs. 18A to 18F are diagrams showing examples of electronic equipment; and

Figs. 19A to 19D are diagrams showing examples of electronic equipment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiment mode

The preferred embodiments of the present invention are explained using Figs. 1 to 8B.

An ICP (inductively coupled plasma) etching device which uses a high density plasma is used in the present invention. Explained simply, the ICP etching device is a device which achieves a plasma density equal to or greater than $10^{11}/cm^3$ by inductively coupling RF power in a plasma at low pressure, and performs etching with a high selectivity and at a high etching rate.

First, the plasma generation mechanism of the ICP dry etching device is explained in detail, using Fig. 4.

A simplified structure diagram of an etching chamber is shown in Fig. 4. An antenna coil 12 is arranged on a quartz substrate 11 in the upper portion of the chamber, and the coil 12 is connected to an RF power source 14 through a matching box 13. Further, an RF power source 17 is connected through a matching box 16 to a lower electrode 15 of a substrate arranged on the opposing side.

If an RF current is applied to the antenna coil 12 over the substrate, then an RF current J flows in the θ direction and a magnetic field B develops in the Z direction.

$$\mu_0 J = \text{rot } B$$

An induced electric field E develops in the θ direction in accordance with Faraday's law of electromagnetic induction.

$$-\partial B/\partial t = \text{rot } E$$

Electrons are accelerated in the θ direction in the induced electric field E and collide with gas molecules, generating a plasma. The direction of the induced electric field is the θ direction, and therefore the probability of electric charge disappearing by charged particles colliding with the etching chamber walls and the substrate is reduced. A high density plasma can therefore be generated at even a low pressure on the order of 1 Pa. Further, there is almost no magnetic field B downstream, and consequently the plasma becomes a high density plasma spread out in a sheet shape.

By regulating the RF power applied to both the antenna coil 12 (ICP power is applied) and the lower electrode 15 of the substrate (bias power is applied), it is possible to control the plasma density and the auto-bias voltage independently. Further, it is possible to vary the frequency of the applied RF power depending on the material of the piece to be processed.

In order to obtain a high density plasma with the ICP etching device, it is necessary for the RF current J to flow with little loss in the antenna coil 12, and in order to make a large surface area, the inductance of the antenna coil 12 must be reduced. An ICP etching device with a multi-spiral coil 22, in which the antenna is partitioned, has therefore been developed, as shown in Fig. 5. Reference numeral 21 denotes a quartz substrate, reference numerals 23 and 26 denote matching boxes, and 24 and 27 denote RF power sources in Fig. 5. Further, a lower electrode 25 for holding a substrate 28 is formed through an insulator 29 in the lower portion of the chamber. If an etching device using ICP in which the multi-

spiral coil is applied is used, then it is possible to preform good etching of the above heat resistant conducting material.

The applicants of the present invention performed several experiments using the multi-spiral ICP etching device (Matsushita Electric model E645) by varying the etching conditions.

The etching test piece used in the experiments is explained first. A base film (200 nm thickness) is formed from a silicon oxynitride film on an insulating substrate (Corning #1737 glass substrate), and a metallic lamination film is formed thereon by sputtering. A tungsten target having a purity equal to or greater than 6N is used. Further, a single gas such as argon (Ar), krypton (Kr), or xenon (Xe), or a mixture of such gasses, may be used. Note that film deposition conditions such as sputtering power, gas pressure, and substrate temperature may be suitably controlled by the operator.

The metallic lamination film has a tungsten nitride film (film thickness: 30 nm) denoted by WN_x (where $0 < x < 1$) as a lower layer, and has a tungsten film (370 nm thickness) as an upper layer.

The metallic lamination film thus obtained contains almost no impurity elements, and in particular, the amount of oxygen contained can be made equal to or less than 30 ppm. The electrical resistivity can be made equal to or less than 20 $\mu\Omega$·cm, typically between 6 and 15 $\mu\Omega$·cm. Further, the film stress can be made from -5×10^9 dyn/cm^2 to 5×10^9 dyn/cm^2.

Note that throughout this specification, a silicon oxynitride film is an insulating film denoted by SiOxNy, and denotes an insulating film containing silicon, oxygen, and nitrogen in predetermined ratios.

Patterning experiments of the metallic lamination film were performed on the etching test piece using the multi-spiral coil ICP etching device. Note that when performing dry etching, it goes without saying that resist is used and patterned into a predetermined shape, forming a resist mask pattern (film thickness: 1.5 μm).

A cross sectional diagram of a model of the etching test piece before etching processing is shown in Fig. 6A. Reference numeral 601 denotes a substrate, reference numeral 602 denotes a base film, 603a and 603b denote a metallic lamination film (film thickness X = 400 nm), and 604a and 604b denote a resist mask pattern (film thickness Y = 1.5 μm) in Fig. 6A. Further, Fig. 6B is a diagram showing the state after etching processing.

Note that, as shown in Fig. 6B, taper angle denotes an angle α between a tapered portion (inclined portion) of the cross sectional shape of the wiring 603 and the base film 602 throughout this specification. Further, the taper angle can be defined as $\tan \alpha = X/Z$, using the width of the tapered portion Z and the film thickness X.

The applicants of the present invention varied several conditions of the dry etching and observed the cross sectional shape of the wiring.

[Experiment 1]

Fig. 1 is a diagram showing the dependence of the taper angle α on the bias power. An experiment was performed with a 13.56 MHz bias power at 20 W, 30 W, 40 W, 60 W, and 100 W; namely, with bias power densities (W/cm^2) of 0.128, 0.192, 0.256, 0.384, and 0.64. Note that the lower electrode was 12.5 cm × 12.5 cm. Further, the resist film thickness was 1.5 μm, the gas pressure was 1.0 Pa, and the gas composition was CF_4 / Cl_2 = 30 / 30 sccm (note that sccm denotes the volume flow rate (cm^3/min) at standard conditions). In addition, the ICP power was 500 W; namely, the ICP power density was 1.02 W/cm^2. Note that, throughout this specification, the value of ICP power divided by ICP area (25 cm diameter) is taken as the ICP power density (W/cm^2).

From Fig. 1, it can be understood that the higher the bias power density, the smaller the taper angle α becomes. Further, by simply regulating the bias power density, the desired taper angle α = 5° to 85° (preferably in the range of 20° to 70°) can be formed.

Note that a SEM photograph of a cross section when the bias power was set to 20 W (bias power density: 0.128 W/cm^2) is shown in Fig. 7A; a SEM photograph of a cross section when the bias power was set to 30 W (bias power density: 0.192 W/cm^2) is shown in Fig. 7B; a SEM photograph of a cross section when the bias power was set to 40 W (bias power density: 0.256 W/cm^2) is shown in Fig. 7C; a SEM photograph of a cross section when the bias power was set to 60 W (bias power density: 0.384 W/cm^2) is shown in Fig. 8A; and a SEM photograph of a cross section when the bias power was set to 100 W (bias power density: 0.64 W/cm^2) is shown in Fig. 8B. It can be observed from each SEM photograph shown in Figs. 7A to 8B that the taper angle α is formed within the range of 20° to 70°, and that the taper angle α can be controlled by changing the bias power density.

It is thought that this is because the selectivity between tungsten and resist becomes small, and a retreating phenomenon of the resist develops.

[Experiment 2]

Fig. 2 is a diagram showing the dependence of the taper angle α on the specific flow rate of CF_4. Experiments were performed with gas composition ratios of CF_4 / Cl_2 = 20 / 40 sccm, 30 / 30 sccm, and 40 / 20 sccm. The gas pressure was 1.0 Pa, the bias power density was 0.128 W/cm^2, the resist film thickness was 1.5 μm, and the ICP power was 500 W (ICP power density: 1.02 W/cm^2).

From Fig. 2, it is understood that the larger the specific flow rate of CF_4, the larger the selectivity between tungsten and resist, and the larger the taper angle α of the wiring becomes. Further, the roughness of the base film becomes less. Regarding the roughness of the base film, it is thought that the reason is due to weak anisotropy of the etching caused by an increase in the flow rate of CF_4 (decrease in the flow rate of Cl_2). Furthermore, by simply regulating the specific flow rate of CF_4, the desired taper angle α = 5° to 85° (preferably in the range of 60° to 80°) can be formed.

[Experiment 3]

An experiment was performed by setting the 13.56 MHz, ICP power to 400 W, 500 W, and 600 W; namely, by setting the ICP power density to 0.82, 1.02, and 1.22. The bias power was 20 W (bias power density: 0.128 W/cm^2), the resist film thickness was 1.5 μm, the gas pressure was 1.0 Pa, and the gas composition was CF_4 / Cl_2 = 30 / 30 sccm.

The etching rate of tungsten becomes larger as the ICP power density gets larger, but the etching rate distribution becomes worse. Further, there are no particular changes seen in the taper angle.

[Experiment 4]

An experiment was performed with gas pressures of 1.0 Pa and 2.0 Pa. The ICP power was 500 W (ICP power density: 1.02 W/cm^2), the gas composition was CF_4 / Cl_2 = 30 / 30 sccm, the bias power was 20 W (bias power density: 0.128 W/cm^2), and the resist film thickness was 1.5 μm.

The tungsten etching rate becomes faster along with higher vacuum, and the anisotropy also becomes stronger. Further, the taper becomes a reverse taper shape at 2.0 Pa.

[Experiment 5]

An experiment was performed with the total flow rate of the etching gas set to 60 sccm and 120 sccm. The gas pressure was 1.0 Pa, the ICP power was 500 W (ICP power density: 1.02 W/cm^2), the gas composition was CF_4 / Cl_2 = 30 / 30 sccm, the bias power was 20 W (bias power density: 0.128 W/cm^2), and the resist film thickness was 1.5 μm.

The etching rate become a little larger for the case of the larger total flow rate of the etching gas.

From the results of the above experiments, it is thought that there is a dependence of the taper angle on the selectivity between tungsten and resist because the taper angle is

mainly influenced by the bias power density conditions. The dependence of the taper angle on the selectivity between tungsten and resist is shown in Fig. 3.

Changes in bias power density have a larger influence on the selectivity between tungsten and resist than on the etching rate of tungsten, and if the bias power density is made large, then there is a tendency for the selectivity between tungsten and resist to fall. The dependence of etching rates of tungsten and resist on bias power density is shown in Fig. 9A, while the dependence of the selectivity between tungsten and resist on bias power density is shown in Fig. 9B.

Namely, as shown in Fig. 6A and in Fig. 6B, resist is etched at the same time as tungsten is etched, and therefore if the selectivity between tungsten and resist is large, the taper angle becomes large, and if the selectivity between tungsten and resist is small, the taper angle becomes small.

Further, if the specific flow rate of CF_4 gas is made smaller in the same way, then there is a tendency for the selectivity between tungsten and resist to fall. Fig. 10A shows the dependance of etching rates of tungsten and resist on specific CF_4 gas flow rate, and Fig. 10B shows the dependence of the selectivity between tungsten and resist on specific CF_4 gas flow rate.

Further, the dependence of etching rates of tungsten and resist on ICP power density is shown in Fig. 11A, and the dependence of the selectivity between tungsten and resist on ICP power density is shown in Fig. 11B.

A test piece in which a base film (200 nm thickness) made from a silicon oxynitride film formed on an insulating substrate, and a metallic lamination film (a lamination film of a tungsten nitride film and a tungsten film) formed on the base film is used as a test piece for etching in each of the above experiments, but with the present invention, it is also possible to apply a thin film, or a lamination structure of a lamination of thin films, selected from the group consisting of a tungsten film, a metallic compound film having a tungsten compound as its main constituent, and a metallic alloy film having a tungsten alloy as its

main constituent. Note, however, that films in which the selectivity with the base film is equal to or less than 2.5, and cases in which the etching rate is extremely small can not be applied. For example, a W-Mo alloy film (having a ratio of W:Mo = 52:48 by weight) possesses a selectivity with the base film (SiO_xN_y) which is equal to or less than approximately 1.5, and the etching rate is small at approximately 50 nm/min, and therefore it is not suitable from a workability standpoint.

A W film is shown as one example here, but for generally known heat resistant conducting materials (such as Ta, Ti, Mo, Cr, Nb, and Si), when an ICP etching device is used, the edge of a pattern can easily be made into a tapered shape. For example, if a Ta film with an etching speed of 140 to 160 nm/min and a selectivity of 6 to 8 is chosen, it has superior values in comparison with the W film having an etching speed of 70 to 90 nm/min and a selectivity of 2 to 4. Therefore, from the standpoint of workability, the Ta film is also suitable, but the Ta film has a resistivity of 20 to 30 $\mu\Omega$cm, which is little high in comparison with the resistivity of the W film, from 10 to 16 $\mu\Omega$cm, and this becomes a problem.

Further, a gas mixture of CF_4 gas and Cl_2 gas is used as the etching gas for the above dry etching, but there are no particular limitations on this, and it is also possible to use a mixed gas of a reactive gas containing fluorine selected from the group consisting of C_2F_6 and C_4F_8, and a gas containing chlorine selected from the group consisting of Cl_2, $SiCl_4$, and BCl_3.

In addition, there are no particular limitations on the etching conditions of the present invention, and for a case of using, for example, an ICP etching device (Matsushita Electric mode: E645) and using carbon tetrafluoride gas (CF_4) and chlorine (Cl_2), the etching conditions may be suitably determined by the operator within the following ranges:

etching gas total flow rate:	60 to 120 sccm
specific etching gas flow rate:	CF_4 / Cl_2 = 30 / 30 sccm to 50 / 10 sccm

gas pressure:	1.0 Pa to 2.0 Pa
(pressure of etching gas atmosphere)	
ICP power density:	0.61 W/cm^2 to 2.04 W/cm^2 (ICP power: 300 W to 1000 W), frequency of 13 MHz to 60 MHz
bias power density:	0.064 W/cm^2 to 3.2 W/cm^2 (bias power: 10 W to 500 W), frequency of 100 kHz to 60 MHz, preferably 6 MHz to 29 MHz
substrate temperature:	0°C to 80°C, preferably 70°C ± 10 °C.

Note that, throughout this specification, the term "electrode" refers to a portion of the term "wiring", and denotes a location for performing electrical connection to another wiring, or a location for intersection with a semiconductor layer. Therefore, for convenience, while the use of "wiring" and "electrode" is properly divided, "wiring" is normally included for sentences using "electrode".

A detailed explanation of the present invention, having the above structure, is made using the embodiments shown below.

[Embodiment 1]

Embodiment 1 of the present invention is explained using Figs. 12 and 13. An active matrix substrate having a pixel TFT and a storage capacitor of a pixel portion, and a driver circuit TFT formed in the periphery of the pixel portion manufactured at the same time, is explained here.

The structure of embodiment 1 has TFTs formed on a substrate 101 having an insulating surface, as shown in Fig. 12. It is preferable to use a glass substrate or a quartz substrate for the substrate 101. It is also possible to use a plastic substrate, provided that the heat resistance is acceptable. In addition, if a reflecting type display device is being

manufactured, then a silicon substrate, a metallic substrate, or a stainless steel substrate, having an insulating film formed on each surface, may also be used as the substrate.

The surface of the substrate 101 on which the TFTs are formed has a base film 102 made from an insulating film containing silicon (a generic name indicating a silicon oxide film, a silicon nitride film, or a silicon oxynitride film throughout this specification). For example, a lamination film of a silicon oxynitride film 102a with a thickness of 10 to 200 nm (preferably between 50 and 100 nm) and manufactured by plasma CVD from SiH_4, NH_3, and N_2O, and a hydrogenated silicon oxynitride film 102b with a thickness of 50 to 200 nm (preferable between 100 and 150 nm) and manufactured similarly from SiH_4, N_2O, and H_2, is formed. A two-layer structure is shown for the base film 102 here, but a single layer insulating film or a lamination film having more than two layers may also be formed.

Further, active layers of the TFTs are formed on the base film 102. A crystalline semiconductor film, obtained from crystallizing a semiconductor film having an amorphous structure, on which patterning is then performed is used as the active layers. A known technique, for example, laser annealing or thermal annealing (solid phase growth methods), rapid thermal annealing (RTA method), or a crystallization method using a catalytic element, in accordance with the technique disclosed in Japanese Patent Application Laid-open No. Hei 7-130652, may be used as the crystallization method. Note that amorphous semiconductor films and microcrystalline semiconductor films exist as semiconductor films having an amorphous structure, and that a compound semiconductor film having an amorphous structure, such as an amorphous silicon germanium film, may also be applied.

A gate insulating film 130 covering the above TFT active layers is formed by using plasma CVD or sputtering from an insulating film containing silicon with a thickness of 40 to 150 nm. A 120 nm thick silicon oxynitride film is formed in embodiment 1. Further, a silicon oxynitride film manufactured by doping O_2 into SiH_4 and N_2O has a reduced fixed electric charge density within the film, and therefore it is a desirable material for use. The

gate insulating film is not limited to this type of silicon oxynitride film, of course, and other insulating films containing silicon may be used in either a single layer or a lamination structure.

A heat resistant conducting material is used for gate electrodes 118 to 122 and a capacitor electrode 123 formed on the gate insulating film, which have a lamination structure of a conducting layer (A) made from a conducting metallic nitride film and a conducting layer (B) made from a metallic film. The conducting layer (B) may be formed from an element selected from the group consisting of Ta, Ti, and W, or from an alloy having one of the above elements as its main constituent, or from an alloy film of a combination of the above elements. In embodiment 1, a conducting lamination film of a 50 nm thick WN film formed as the conducting layer (A) and a 250 nm thick W film formed as the conducting layer (B) by sputtering which uses a W target having a purity of 6 N and in which Ar gas and nitrogen (N_2) gas is introduced, is patterned, completing the gate electrodes 118 to 122 and the capacitor electrode 123. Note that etching is performed so that a tapered portion is formed in the edges of the gate electrodes 118 to 123. The etching process is performed using an ICP etching device. Details of this technique are as shown in the embodiment mode of the present invention. In embodiment 1, etching is performed using a gas mixture of CF_4 and Cl_2 for the etching gas, with the flow rates each to 30 sccm, the ICP power density set to 3.2 W/cm^2 (frequency: 13.56 MHz), the bias power density set to 0.224 W/cm^2 (frequency: 13.56 MHz), and a gas pressure of 1.0 Pa. By using these etching conditions, a tapered portion is formed in the edge portions of the gate electrodes 118 to 122 and the capacitor electrode 123, in which the thickness increases gradually from the edge portion toward the inside. The angle can be made from 25 to 35°, preferably 30°.

Note that, in order to perform etching so as not to leave any residue when forming the gate electrodes 118 to 122 and the capacitor electrode 123 which have the tapered shape, overlap etching is performed, in which the etching time is increased on the order of 10 to

20%, and therefore the gate insulating film 130 has a portion which becomes thin in practice.

Further, in embodiment 1, in order to form LDD regions, an impurity element for imparting n-type or p-type conductivity is added into the active layers in a self-aligning manner by ion doping with the gate electrodes 118 to 122 having the tapered portions in their edges, as masks. Furthermore, in order to form suitable, desired LDD regions, an impurity element for imparting n-type or p-type conductivity is added to the active layers by ion doping with a resist pattern as a mask.

A structure having a channel forming region 206, an LDD region 207 overlapping with the gate electrode, a source region 208 composed of a high concentration p-type impurity region, and a drain region 209 in the active layer is thus formed in a first p-channel TFT (A) 200a of the driver circuit. A first n-channel TFT (A) 201a has a channel forming region 210, an LDD region 211 made from a low concentration n-type impurity region overlapping the gate electrode 119, a source region 212 formed by a high concentration n-type impurity region, and a drain region 213 in the active layer. The LDD region overlapping the gate electrode 119, taken as L_{ov}, has a length of 0.1 to 1.5 μm, preferably between 0.3 and 0.8 μm, in the longitudinal direction of the channel for a channel length of 3 to 7 μm. The length of L_{ov} controls the thickness of the gate electrode 119 and the angle of the tapered portion.

Further, the active layer in a second p-channel TFT (A) 202a of the driver circuit similarly has a channel forming region 214, an LDD region 215 overlapping the gate electrode 120, a source region 216 formed by a high concentration p-type impurity region, and a drain region 217 in the active layer. In a second n-channel TFT (A) 203a, the active layer has a channel forming region 218, an LDD region 219 overlapping the gate electrode 121, a source region 220 formed by a high concentration n-type impurity region, and a drain region 221. The LDD region 219 has the same structure as the LDD region 211. A pixel TFT 204 has channel forming regions 222a and 222b, LDD regions 223a and 223b formed

by low concentration n-type impurity regions, and source or drain regions 225 to 227 formed by high concentration n-type impurity regions in the active layer. The LDD regions 223a and 223b have the same structure as the LDD region 211. In addition, a storage capacitor 205 is formed from the capacitor wiring 123, the gate insulating film, and semiconductor layers 228 and 229 connected to the drain region 227 of the pixel TFT 204. In Fig. 12, the n-channel TFT and the p-channel TFT of the driver circuit have a single gate structure in which one gate electrode is provided between the source and drain pair, and the pixel TFT has a double gate structure, but all of the TFTs may be given a single gate structure, and a multi-gate structure in which a plurality of gate electrodes are provided between one source and drain pair will not cause any hindrance.

Further, there is a protecting insulating film 142 covering the gate electrode and the insulating film 130. The protecting insulating film may be formed by a silicon oxide film, a silicon oxynitride film, a silicon nitride film, or by a lamination film of a combination of these films.

In addition, there is an interlayer insulating film 143 made from an organic insulating material covering the protecting insulating film 142. Materials such as polyimide, acrylic, polyamide, polyimide amide, and BCB (benzocyclobutene) can be used as an organic resin material.

Moreover, there are source wirings and drain wirings on the interlayer insulating film 143 for connecting to the source regions and drain regions formed on the respective active layers, through contact holes. Note that the source wirings and the drain wirings have a lamination structure of a lamination film of Ti and aluminum, denoted by reference numerals 144a to 154a, and a transparent conducting film, denoted by reference numerals 144b to 154b. Further, the drain wirings 153a and 153b also function as pixel electrodes. An indium oxide and zinc oxide alloy (In_2O_3 - ZnO) and zinc oxide (ZnO) are suitable materials for the transparent conducting film, and in order to additionally increase the transmissivity and the conductivity, materials such as zinc oxide in which gallium (Ga) has

been added (ZnO:Ga) can be ideally used.

With the above construction, the structure of TFTs constituting each circuit is optimized in accordance with the specifications required by the pixel TFT and the driver circuit, and it is possible to increase the operating performance and the reliability of a semiconductor device. In addition, by forming the gate electrodes with a conducting material having heat resistance, the activation of the LDD regions and the source regions or drain regions becomes easy.

Additionally, during formation of the LDD region overlapping the gate electrode through the gate insulating film, by forming the LDD region which possesses a concentration gradient of an impurity element added with the aim of controlling the conductivity type, it can be expected that the electric field relaxation effect will be increased, particularly in the vicinity of the drain region.

The active matrix substrate shown in Fig. 12 can be applied as is to a transmitting type liquid crystal display device.

An active matrix type liquid crystal display device, in which the active matrix substrate shown in Fig. 12 is applied, is explained next using Fig. 13.

First, a resin film on the active matrix substrate is patterned, forming rod shape spacers 405a to 405e and 406. The placement of the spacers may be arbitrarily determined. Note that a method of forming the spacers by dispersing grains of several μm may also be used.

An alignment film 407 is formed next in the pixel portion of the active matrix substrate from a material such as a polyimide resin in order to orient the liquid crystals. After forming the alignment film, a rubbing process is performed, orienting the liquid crystal molecules so as to possess a certain fixed pre-tilt angle.

A light shielding film 402, a transparent conducting film 403, and an alignment film 404 are formed in an opposing substrate 401 on the opposite side. The light shielding film 402 is formed with a thickness of 150 to 300 nm by a film such as a Ti film, a Cr film, or

an Al film. The active matrix substrate, on which the pixel portion and the driver circuit are formed, and the opposing substrate are then joined together by a sealing member 408.

Afterward, a liquid crystal material 409 is injected between both substrates. A known liquid crystal material may be used for the liquid crystal material. For example, in addition to a TN liquid crystal, a thresholdless antiferroelectric mixed liquid crystal, indicating an electro-optical response in which the transmissivity changes continuously with respect to an electric field, can also be used. V-shape electro-optical response characteristics are displayed in some thresholdless antiferroelectric mixed liquid crystal. The reflecting type active matrix type liquid crystal display device shown in Fig. 13 is thus completed.

[Embodiment 2]

Using Fig. 14, embodiment 2 shows an example of manufacturing a display device using a bottom gate TFT which differs from embodiment 1 (a top gate TFT) above.

First, a metallic lamination film is formed by sputtering on an insulating substrate 1801. The metallic lamination film has a tungsten nitride film for a bottom layer and a tungsten film for a top layer. Note that a base film contacting the substrate may also be formed, from a film such as a silicon oxynitride film denoted by SiO_xN_y. Next, a resist mask for obtaining a desired gate wiring pattern is formed by photolithography.

It is necessary for constituents such as a gate insulating film and a channel forming region to be formed on the gate wiring in the bottom gate TFT. In order to increase the characteristics of the bottom gate structure TFT, the coverage of the films formed on the gate wiring, and the voltage resistance of the gate insulating film, it is preferable that the taper angle of gate wirings 1802 to 1805 be equal to or less than 60°, more preferably equal to or less than 40°.

Next, as shown above in the embodiment mode of the present invention, the taper angle of the gate wirings 1802 to 1805 is made equal to or less than 60°, more preferably equal to or less than 40°, using an ICP etching device and selecting suitably the bias power

and the specific gas flow rate. Known techniques may be used for subsequent processing, and there are no particular limitations imposed.

In Fig. 14, reference numeral 1814 denotes a CMOS circuit, reference numeral 1815 denotes an n-channel TFT, 1816 denotes a pixel TFT, 1817 denotes an interlayer insulating film, 1818a denotes a pixel electrode, and 1818b denotes an ITO film. The ITO film 1818b is formed in order to be connected to an external terminal such as an FPC 1823 through adhesive 1822. Further, reference numeral 1819 denotes a liquid crystal material, and 1820 denotes an opposing electrode. In addition, reference numeral 1801 denotes the first substrate, 1808 denotes a sealing region, 1807, and 1809 to 1812 denote rod shape spacers, and 1821 denotes a second substrate.

Note that it is possible to freely combine embodiment 2 with embodiment 1.

[Embodiment 3]

Examples of various wiring structures formed on an insulating surface by utilizing the present invention are shown in Figs. 15A to 15F. A cross sectional diagram of a single layer structure wiring made from a material 1501 having tungsten as its main constituent and formed on a film (or a substrate) 1500 having an insulating surface is shown in Fig. 15A. This wiring is formed by patterning a film formed by sputtering which uses a target with a purity of 6N (99.9999%) and a single gas, argon (Ar), as the sputtering gas. Note that the stress is controlled by setting the substrate temperature equal to or less than 300°C, and by setting the sputtering gas pressure equal to or greater than 1.0 Pa, and that other conditions (such as the sputtering power) may be suitably determined by the operator.

When performing the above patterning, a taper angle α is controlled by the method shown in the embodiment mode of the present invention, in accordance with the bias power density, for example.

The cross sectional shape of the wiring 1501 thus obtained has the desired taper angle α. Further, there are almost no impurity elements contained in the wiring 1501, and in

particular, the amount of oxygen contained can be made equal to or less than 30 ppm, and the electrical resistivity can be made equal to or less than 20 $\mu\Omega$·cm, typically between 6 $\mu\Omega$·cm and 15 $\mu\Omega$·cm. Further, the film stress can be controlled within the range of -5×10^{10} to 5×10^{10} dyn/cm^2.

Fig. 15B shows a two-layer structure, similar to the gate electrode of embodiment 1. Note that tungsten nitride (WN_x) is taken as the lower layer, and that tungsten is taken as the upper layer. Also note that the thickness of a tungsten nitride film 1502 may be set from 10 to 50 nm (preferably between 10 and 30 nm), and that the thickness of a tungsten film 1503 may be set from 200 to 400 nm (preferably between 250 and 350 nm). The two films are laminated in succession, without exposure to the atmosphere, using sputtering in embodiment 3.

Fig. 15C is an example of covering a wiring 1504, made from a material having tungsten as its main constituent and formed on the film (or substrate) 1500 which possesses an insulating surface, by an insulating film 1505. The insulating film 1505 may be formed by a silicon nitride film, a silicon oxide film and a silicon oxynitride film SiO_xN_y (where $0 < x$, and $y < 1$), or by a lamination film of a combination of these films.

Fig. 15D is an example of covering the surface of a wiring 1506 made from a material having tungsten as its main constituent, and formed on the film (or substrate) 1500 having an insulating surface, by a tungsten nitride film 1507. Note that if a nitrating process, such as plasma nitrating, is performed on the wiring in the state of Fig. 15A, then the structure of Fig. 15D can be obtained.

Fig. 15E is an example of surrounding a wiring 1509 made from a material having tungsten as its main constituent, and formed on the film (or substrate) 1500 having an insulating surface, by tungsten nitride films 1510 and 1508. Note that if a nitrating process, such as plasma nitrating, is performed on the wiring in the state of Fig. 15B, then the structure of Fig. 15E can be obtained.

Fig. 15F is an example of covering by an insulating film 1511, after forming the state

of Fig. 15E. The insulating film 1511 may be formed by a silicon nitride film, a silicon oxide film, a silicon oxynitride film, or a lamination film of a combination of these films.

The present invention can thus be applied to various wiring structures. It is possible to freely combine the constitution of embodiment 3 with the constitutions shown in embodiment 1 and in embodiment 2.

[Embodiment 4]

A case of applying the present invention to a reflection type liquid crystal display device manufactured over a silicon substrate is explained in Embodiment 4. As a substitute for the active layer comprising a crystalline silicon film in Embodiment 1, an impurity element for imparting n-type or p-type conductivity is added directly into a silicon substrate (silicon wafer), and the TFT structure may be realized. Further, the structure is reflection type, and therefore a metallic film having a high reflectivity (for example, aluminum, silver, or an alloy of these (an Al-Ag alloy)) and the like may be used as a pixel electrode.

Note that it is possible to freely combine the constitution of Embodiment 4 with the constitution of any of embodiments 1 to 3.

[Embodiment 5]

It is possible to use the present invention when forming an interlayer insulating film over a conventional MOSFET, and then forming a TFT on that. In other words, it is possible to realize a semiconductor device with a three dimensional structure. Further, it is possible to use an SOI substrate such as SIMOX, Smart-Cut (a trademark of SOITEC corporation), or ELTRAN (a trademark of Cannon, Inc.)

Note that it is possible to freely combine the structure of embodiment 5 with the structure of any of embodiments 1 to 4.

[Embodiment 6]

It is possible to apply the present invention to an active matrix EL display. An example of this is shown in Fig. 16.

Fig. 16 is a circuit diagram of an active matrix EL display. Reference numeral 81 denotes a pixel portion, and an x-direction driver circuit 82 and a y-direction driver circuit 83 are formed in its peripheral. Further, each pixel in the pixel portion 81 comprises a switching TFT 84, a capacitor 85, a current controlling TFT 86, and an organic EL element 87, and the switching TFT 84 is connected to x-direction signal lines 88a (or 88b) and to y-direction signal lines 89a (or 89b, 89c). Furthermore, power supply lines 90a and 90b are connected to the current controlling TFT 86.

In an active matrix EL display of the present embodiment, TFTs used in an x-direction driver circuit 82, a y-direction driver circuit 83 and current controlling TFT 86 are formed by combining p-channel TFT 200a or 202a of Fig. 12 and n-channel TFT 201a or 203a of Fig. 12. The TFTs for switching TFT 84 are formed by n-channel TFT 204 of Fig. 12.

It is possible to freely combine the active matrix EL display of the present invention with any constitution of Embodiments 1 to 5.

[Embodiment 7]

The structure of the active matrix liquid crystal display device shown in Fig. 13 of the Embodiment 1 is described with reference to the perspective view of Fig. 17. The active matrix substrate (the first substrate) comprises a pixel portion 802, a gate side driver circuit 803 and a source side driver circuit 804 formed over a glass substrate 801. The pixel TFT 805 of the pixel portion (corresponding to pixel TFT 204 of Fig. 13) is an n-channel TFT, and is connected to a pixel electrode 806 and a storage capacitor 807 (corresponding to storage capacitor 205 of Fig. 13).

The driver circuits disposed in the periphery are comprised of a CMOS circuit as its base. The gate side driver circuit 803 and the source side driver circuit 804 are connected to the pixel portion 802 through the gate wiring 808 and the source wiring 809 respectively.

Further, input-output wiring (connecting wiring) 812 and 813 are disposed in the external input-output terminal 811 connected to the FPC 810 for transmitting signals to the driver circuits. Reference numeral 814 is an opposing substrate (the second substrate).

Note that though the semiconductor device shown in Fig. 17 is referred to as active matrix liquid crystal display device in this Specification, the liquid crystal panel furnished with an FPC as shown in Fig. 17 is referred to as a liquid crystal module in general. Accordingly it is acceptable to refer an active matrix liquid crystal display device of this Embodiment as a liquid crystal module.

[Embodiment 8]

TFTs manufactured by implementing the present invention can be used for various electro-optical devices. Namely the present invention can be applied to all those electronic appliances that incorporate such an electro-optical device as the display section.

Examples of the electronic appliances include a video camera, a digital camera, a head mounted display (a goggle type display), a wearable display, a car navigation system, a personal computer and a portable information terminal (a mobile computer, a cellular telephone, an electronic book). Fig. 18A to 18F show examples of these.

Fig. 18A shows a personal computer, which comprises: a main body 2001; an image input section 2002; a display section 2003; and a keyboard 2004. The present invention can be applied to the image input section 2002, the display section 2003 or other signal driver circuits.

Fig. 18B shows a video camera, which comprises: a main body 2101; a display section 2102; a sound input section 2103; an operation switch 2104; a battery 2105; and an image receiving section 2106. The present invention can be applied to the display section 2102, the sound input section 2103 or other signal control circuits.

Fig. 18C shows a mobile computer, which comprises: a main body 2201; a camera section 2202; an image receiving section 2203; an operation switch 2204; and a display

section 2205. The present invention can be applied to the display section 2205 or other signal driver circuits.

Fig. 18D shows a goggle type display, which comprises: a main body 2301; a display section 2302; and an arm section 2303. The present invention can be applied to the display section 2302 or other signal driver circuits.

Fig. 18E shows a player that uses a recording medium storing a program (hereinafter called the "recording medium"). It comprises a main body 2401, a display section 2402, a speaker unit 2403, a recording medium 2404 and an operation switch 2405. Note that by using DVD (digital versatile disc), CD, etc., as a recording medium of this device, music appreciation, film appreciation, games or the use for Internet can be performed. The present invention can be applied to the display device 2402 and other signal driver circuits.

Fig. 18F shows a digital camera, which comprises: a main body 2501; a display section 2502; a view finder section 2503; an operation switch 2504; and an image reception unit (not shown). The present invention can be applied to the display unit 2502 or other signal driver circuits.

As described above, the applicable range of the present invention is very large, and it can be applied to electronic appliances of various fields. Further, the electronic appliances of the present Embodiment can be realized by using constitution of any combination of Embodiments 1 to 7.

[Embodiment 9]

TFTs manufactured by implementing the present invention can be used for various electro-optical devices. Namely the present invention can be applied to all those electronic appliances that incorporate such an electro-optical device as the display section.

Projectors (rear type or front type) or the like can be given as such electronic appliances. The examples are shown in Figs. 19A to 19D.

Fig. 19A shows a front type projector, which comprises: a projection system 2601; and a screen 2602. The present invention can be applied to a liquid crystal display device 2808 which forms a part of the projection system 2601, or other signal driver circuits.

Fig. 19B shows a rear type projector, which comprises: a main body 2701; a projection system 2702; a mirror 2703; and a screen 2704. The present invention can be applied to the liquid crystal display device 2808 that constitutes a part of the projection system 2702, or other signal driver circuit.

Note that Fig. 19C shows an example of the construction of the display devices 2601 and 2702 in Figs. 19A and 19B. The projection systems 2601 and 2702 comprise: a light source optical system 2801; mirrors 2802, 2804 to 2806; a dichroic mirror 2803; a prism 2807; a liquid crystal display device 2808; a phase difference plate 2809; and a projection optical system 2810. The projection optical system 2810 comprises an optical system including a projection lens. Though the present Embodiment shows an example of the three-plate system, there is no limitation to such a system, but may be applied to a single-plate optical system. The operator may appropriately dispose an optical lens, a film having a polarization function, a film for adjusting the phase, an IR film, etc, in the optical path indicated by an arrow in Fig. 19C.

Fig. 19D shows an example of the structure of light source optical system 2801 in Fig. 19C. In this embodiment, the light source optical system 2801 comprises: a reflector 2811; a light source 2812; lens arrays 2813 and 2814; a polarization conversion element 2815; and a condenser lens 2816. Incidentally, the light source optical system shown in Fig. 19D is an example but is in no way restrictive. For example, the operator may appropriately dispose an optical lens, a film having a polarization function, a film for adjusting the phase, an IR film, etc, in the light source optical system.

As described above, the applicable range of the present invention is very large, and it can be applied to electronic appliances of various fields. Further, the electronic appliances of the present Embodiment can be realized by using constitution of any

combination of Embodiments 1 to 3 and 7. Provided, however the projectors of the present Embodiment is a transmission type liquid crystal display device and it is needless to say that they cannot be applied to a reflection type liquid crystal display devices.

By suitably setting the conditions of bias power and specific gas flow rate, which are capable of controlling a taper angle α of a wiring, the selectivity with respect to a base film can be increased and at the same time, the desired taper angle α can be obtained in accordance with the present invention. As a result, the coverage of films formed on the wiring becomes better, and therefore, defects such as wiring chipping, wiring breakage, and short circuits can be reduced.

Further, etching can be performed with good distribution within the section, and a uniform wiring shape can be obtained.

Furthermore, the present invention can be applied to the opening processes of a contact hole etc.

WHAT IS CLAIMED IS:

1. A wiring comprising a tungsten film, a metallic compound film having a tungsten compound as its main constituent, or a metallic alloy film having a tungsten alloy as its main constituent, wherein a taper angle α of said wiring is in a range from 5° to 85°.

2. A wiring comprising a lamination structure of laminated thin films selected from the group consisting of: a tungsten film; a metallic compound film having a tungsten compound as its main constituent; and a metallic alloy film having a tungsten alloy as its main constituent, wherein a taper angle α of said wiring is in a range from 5° to 85°.

3. The wiring according to claim 1 or 2, wherein said metallic alloy film is an alloy film of one element, or a plurality of elements, selected from the group consisting of Ta; Ti; Mo; Cr; Nb; and Si, and tungsten.

4. The wiring according to claim 1 or 2, wherein said metallic compound film is a nitride film of tungsten.

5. The wiring according to claim 2, wherein a lowest layer of said wiring is a silicon film having a conductivity.

6. A semiconductor device comprising a wiring made from a tungsten film, a metallic compound film having a tungsten compound as its main constituent, or a metallic alloy film having a tungsten alloy as its main constituent, wherein a taper angle α of said wiring is in a range from 5° to 85°.

7. A semiconductor device comprising a wiring made from a lamination structure of laminated thin films selected from the group consisting of: a tungsten film; a metallic compound film having a tungsten compound as its main constituent; and a metallic alloy film having a tungsten alloy as its main constituent, wherein a taper angle α of said wiring is in a range from 5° to 85°.

8. The semiconductor device according to claim 6 or 7, wherein said wiring is a gate wiring of a thin film transistor.

9. The semiconductor device according to claim 6 or 7, wherein said semiconductor device is an active matrix type liquid crystal display device.

10. The semiconductor device according to claim 6 or 7, wherein said semiconductor device is an EL display device.

11. The semiconductor device according to claim 6 or 7, wherein said semiconductor device is one selected from the group consisting of a video camera, a digital camera, a projector, a goggle type display, a car navigation system, a personal computer, or a portable information terminal.

12. A semiconductor device comprising:

a semiconductor layer over a substrate, said semiconductor layer comprising a lightly doped region adjacent to a channel forming region in said semiconductor layer; and

a gate electrode adjacent to said semiconductor layer with a gate insulating film interposed therebetween,

wherein said gate electrode comprises a tungsten film, a metallic compound film having a tungsten compound as its main constituent, or a metallic alloy film having a

tungsten alloy as its main constituent, wherein a taper angle α of said gate electrode is in a range from 5° to 85°.

13. The semiconductor device according to claim 12, wherein said semiconductor device is an active matrix type liquid crystal display device.

14. The semiconductor device according to claim 12, wherein said semiconductor device is an EL display device.

15. The semiconductor device according to claim 12, wherein said semiconductor device is one selected from the group consisting of a video camera, a digital camera, a projector, a goggle type display, a car navigation system, a personal computer, or a portable information terminal.

16. A method of forming a wiring comprising the steps of:

forming a metallic thin film on a base film;

forming a resist pattern on said metallic thin film; and

forming said wiring by performing an etching of said metallic thin film having said resist pattern,

wherein a taper angle α of said wiring is controlled in accordance with a bias power density of an ICP etching device.

17. A method of forming a wiring comprising the steps of:

forming a metallic thin film on a base film;

forming a resist pattern on said metallic thin film; and

forming said wiring by performing an etching of said metallic thin film having said resist pattern,

wherein a taper angle α of said wiring is controlled in accordance with a flow rate of a gas containing fluorine.

18. The method of forming a wiring according to claim 16 or 17, wherein said etching is performed using an etching gas comprising a mixed gas of a first reaction gas containing fluorine and a second reaction gas containing chlorine, and a specific selectivity in said etching gas between said base film and said metallic thin film is 2.5 or more.

19. The method of forming a wiring according to claim 16 or 17, wherein said metallic thin film is a thin film, or a lamination film of thin films, selected from the group consisting of: a tungsten film; a metallic compound film having a tungsten compound film as its main constituent; and a metallic alloy film having a tungsten alloy as its main constituent.

20. A method of dry etching comprising a removal by an etching gas of a desired portion of a thin film selected from the group consisting of: a tungsten film; a metallic compound film having a tungsten compound film as its main constituent; and a metallic alloy film having a tungsten alloy as its main constituent, wherein said etching gas is a mixed gas of a first reaction gas containing fluorine and a second reaction gas containing chlorine.

21. The method of dry etching according to claim 20, wherein said first reaction gas is a gas selected from the group consisting of CF_4, C_2F_6, and C_4F_8.

22. The method of dry etching according to claim 20, wherein said second reaction gas is a gas selected from the group consisting of Cl_2, $SiCl_4$, and BCl_3.

23. The method of dry etching according to claim 20, wherein said method of dry etching uses an ICP etching device.

24. The method of dry etching according to claim 20, wherein a taper angle α of said wiring is controlled in accordance with a bias power density of said ICP etching device.

25. A method of dry etching wherein a taper angle of an inside sidewall of a hole or a recess formed by said etching is controlled in accordance with a bias power density.

26. A method of dry etching wherein a taper angle of an inside sidewall of a hole or a recess formed by said etching is controlled in accordance with a specific gas flow rate.

27. The method of dry etching according to claim 25 or 26, wherein said method of dry etching uses an ICP etching device.

28. A method of manufacturing a semiconductor device comprising the steps of:

forming a semiconductor layer over a substrate, said semiconductor layer comprising a lightly doped region adjacent to a channel forming region in said semiconductor layer;

forming a metallic thin film over a substrate;

forming a resist pattern on said metallic thin film; and

etching said metallic thin film having said resist pattern, thereby to form a gate electrode of a thin film transistor,

wherein said gate electrode comprises a tapered shape having an taper angle from 5° to 85°.

29. The method of manufacturing a semiconductor device according to claim 28, wherein said semiconductor device is an active matrix type liquid crystal display device.

30. The method of manufacturing a semiconductor device according to claim 28, wherein said semiconductor device is an EL display device.

31. The method of manufacturing a semiconductor device according to claim 28, wherein said semiconductor device is one selected from the group consisting of a video camera, a digital camera, a projector, a goggle type display, a car navigation system, a personal computer, or a portable information terminal.

ABSTRACT OF THE DISCLOSURE

A dry etching method for forming tungsten wiring having a tapered shape and having a large specific selectivity with respect to a base film is provided. If the bias power density is suitably regulated, and if desired portions of a tungsten thin film are removed using an etching gas having fluorine as its main constituent, then the tungsten wiring having a desired taper angle can be formed.

Fig. 1

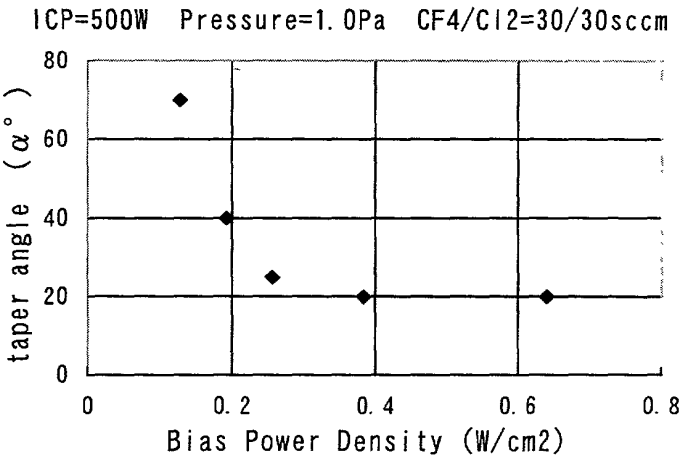

ICP=500W Pressure=1.0Pa CF4/Cl2=30/30sccm
taper angle (α°)
80
60
40
20
0
0
0.2
0.4
0.6
0.8
Bias Power Density (W/cm2)

Fig. 2

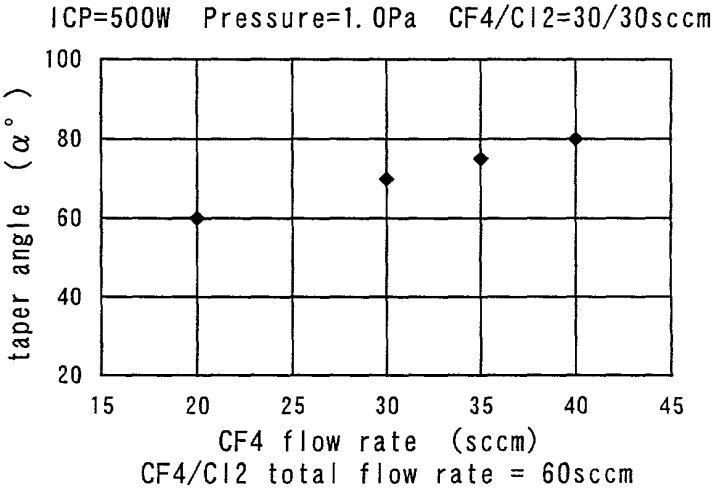

ICP=500W Pressure=1.0Pa CF4/Cl2=30/30sccm
taper angle (α°)
100
80
60
40
20
15
20
25
30
35
40
45
CF4 flow rate (sccm)
CF4/Cl2 total flow rate = 60sccm

Fig. 3

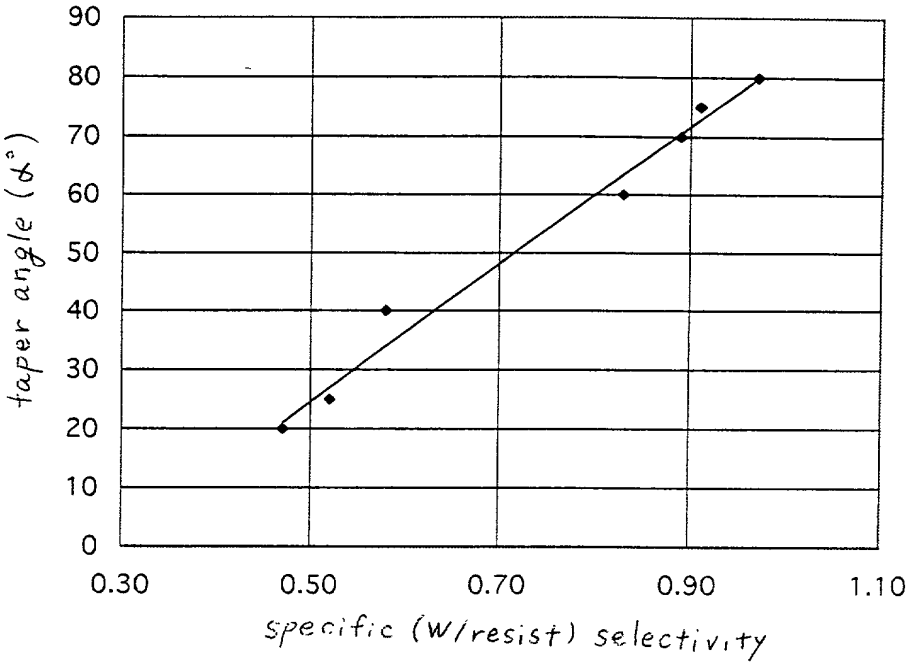

90
80
70
60
50
40
30
20
10
0
taper angle (α°)
0.30
0.50
0.70
0.90
1.10
specific (W/resist) selectivity

Fig. 4

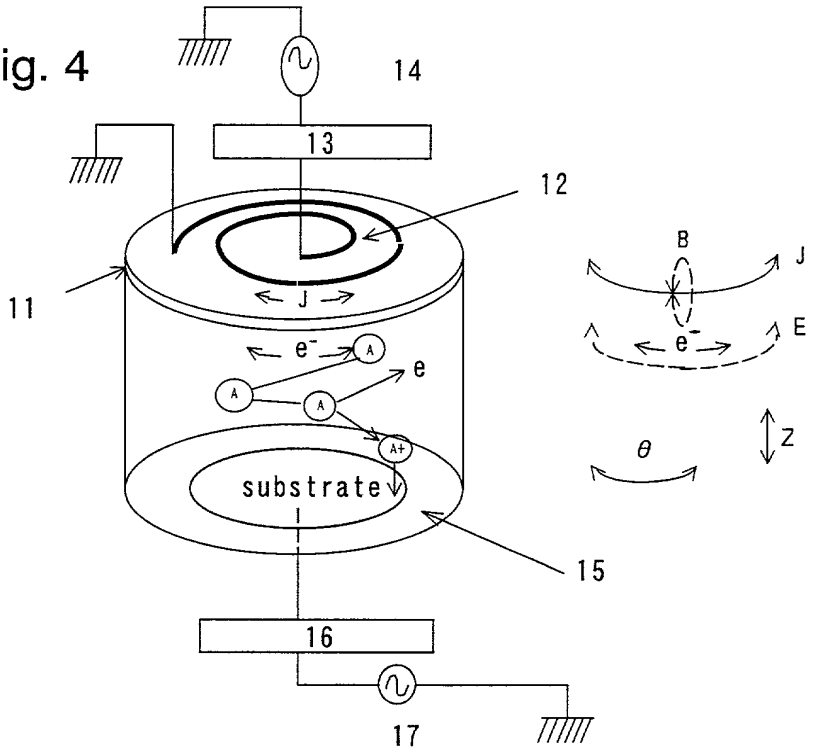


Fig. 5

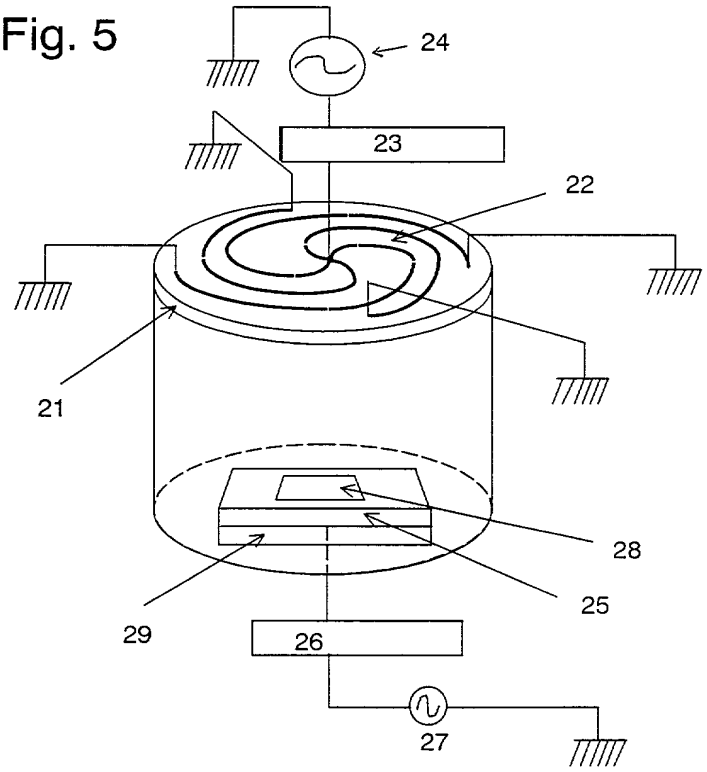


Fig. 6A

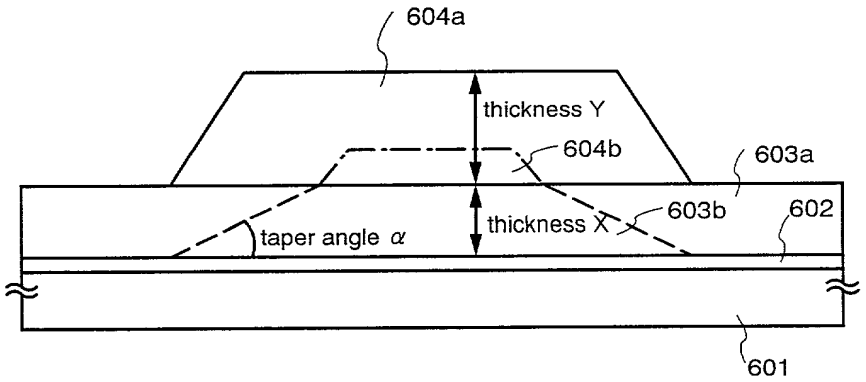

604a
thickness Y
604b
603a
thickness X
603b
602
taper angle α
601

Fig. 6B

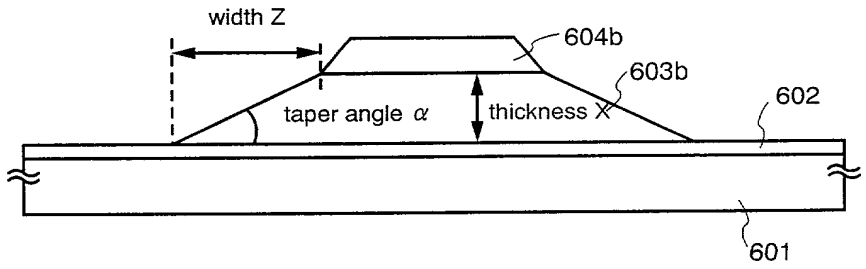
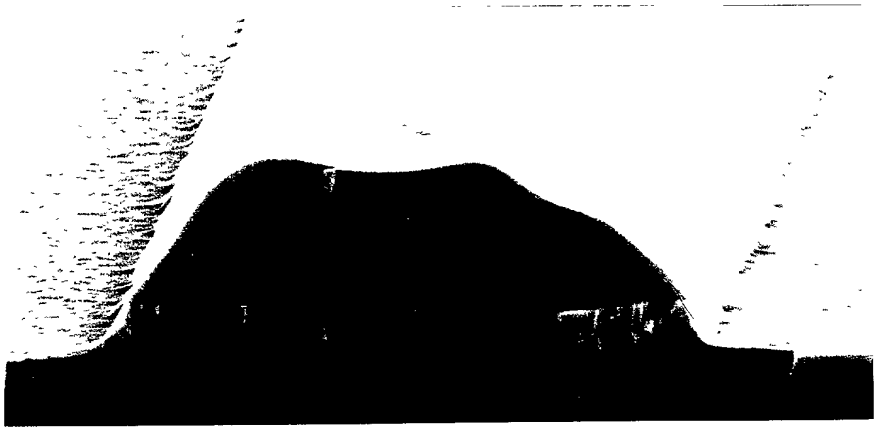

width Z
604b
603b
602
taper angle α
thickness X
601

Fig. 7A



Bias Power:20W

Fig. 7B

Bias Power:30W

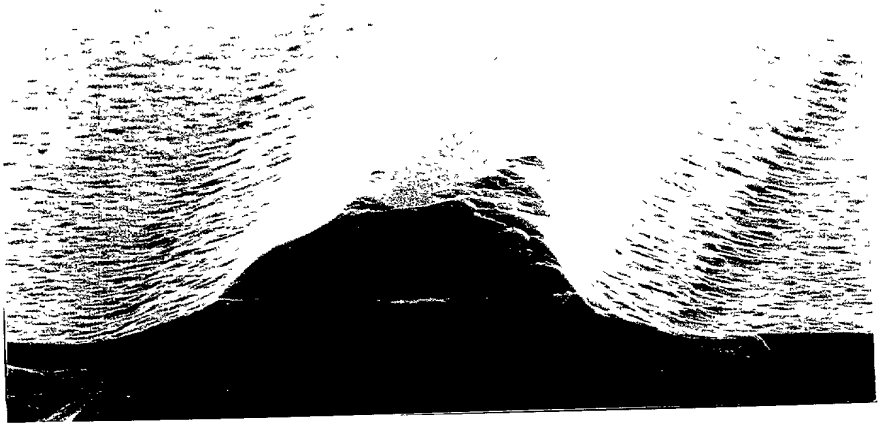
Fig. 7C

Bias Power:40W

Fig. 8A

Bias Power:60W

Fig. 8B



Bias Power:100W

X15.0K 2.00μm

Fig. 9A

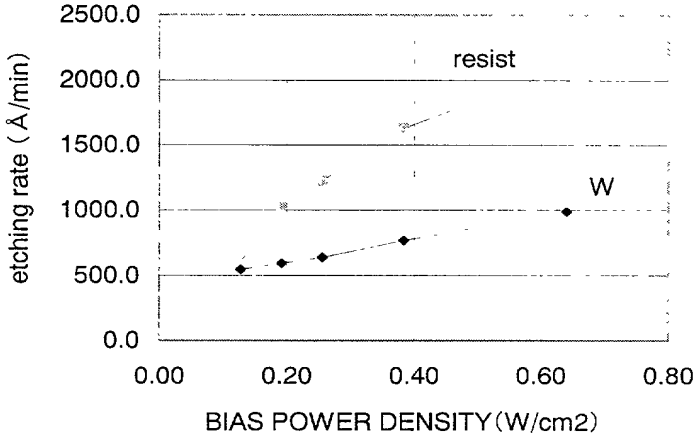

2500.0
2000.0
1500.0
1000.0
500.0
0.0
etching rate (Å/min)
resist
W
0.00
0.20
0.40
0.60
0.80
BIAS POWER DENSITY(W/cm2)

Fig. 9B

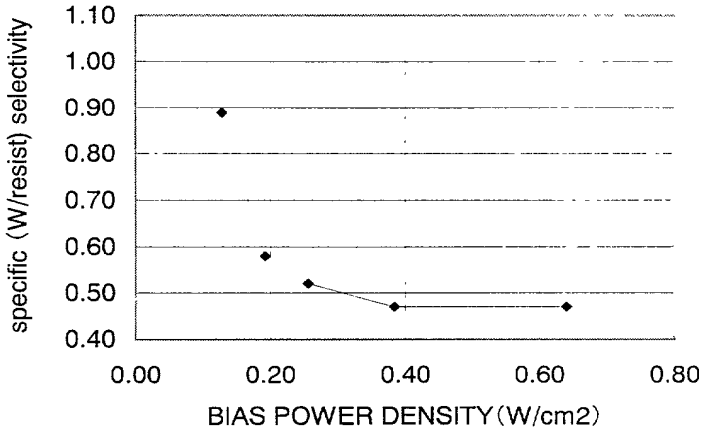

1.10
1.00
0.90
0.80
0.70
0.60
0.50
0.40
specific (W/resist) selectivity
0.00
0.20
0.40
0.60
0.80
BIAS POWER DENSITY(W/cm2)

Fig. 10A

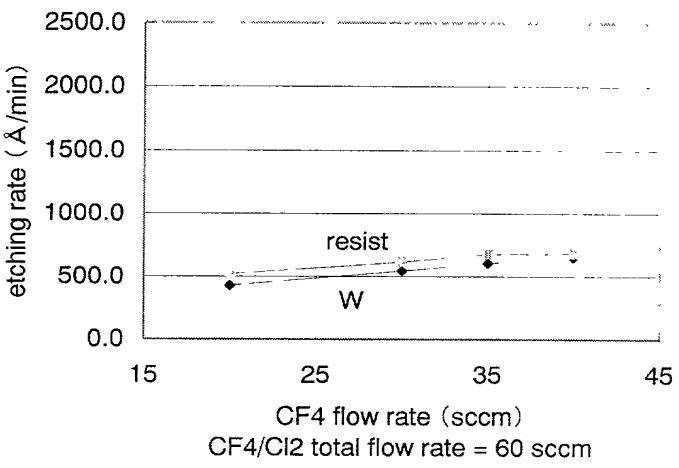


Fig. 10B

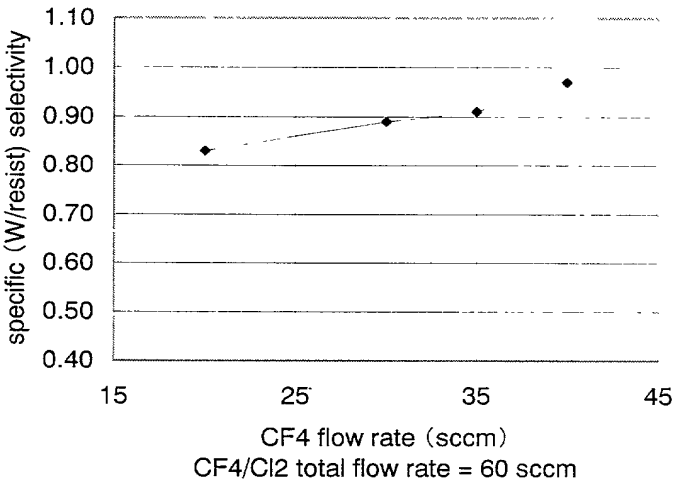


Fig. 11A

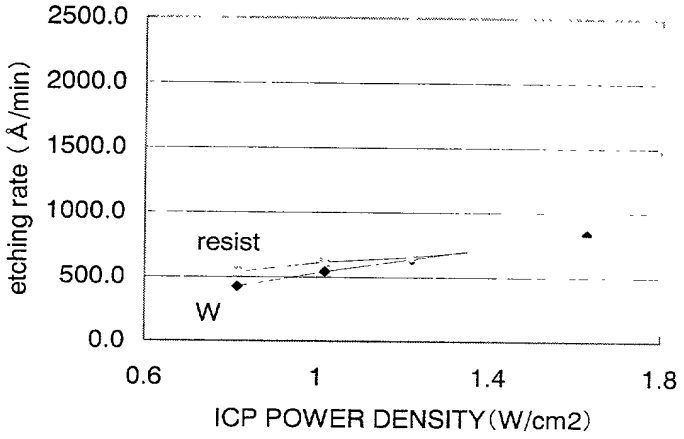


Fig. 11B

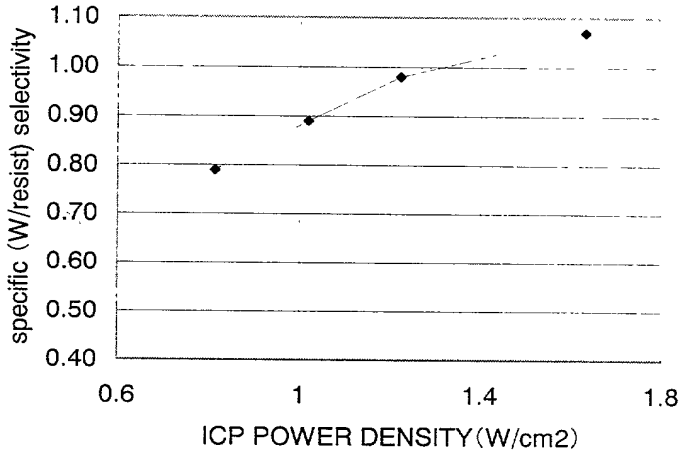


Fig. 12

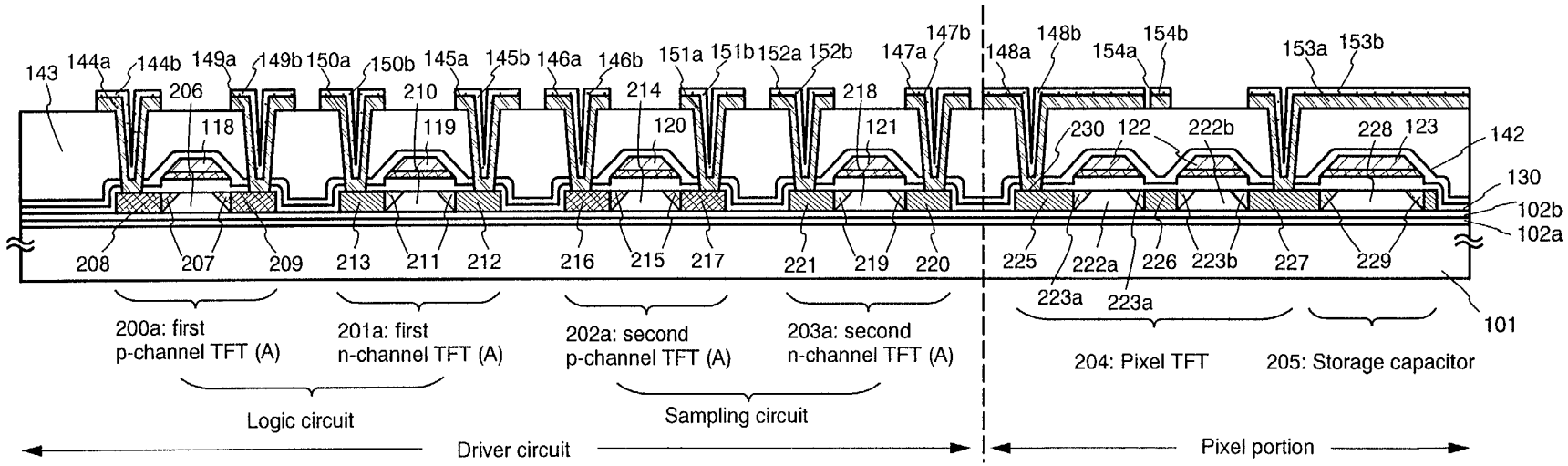

143
144a
144b
149a
149b
150a
150b
145a
145b
146a
146b
151a
151b
152a
152b
147a
147b
148a
148b
154a
154b
153a
153b
206
210
214
218
118
119
120
121
230
122
222b
228
123
142
130
102b
102a
208
207
209
213
211
212
216
215
217
221
219
220
225
222a
226
223b
227
229
223a
223a
101
200a: first p-channel TFT (A)
201a: first n-channel TFT (A)
202a: second p-channel TFT (A)
203a: second n-channel TFT (A)
204: Pixel TFT
205: Storage capacitor
Logic circuit
Sampling circuit
Driver circuit
Pixel portion

Fig. 13

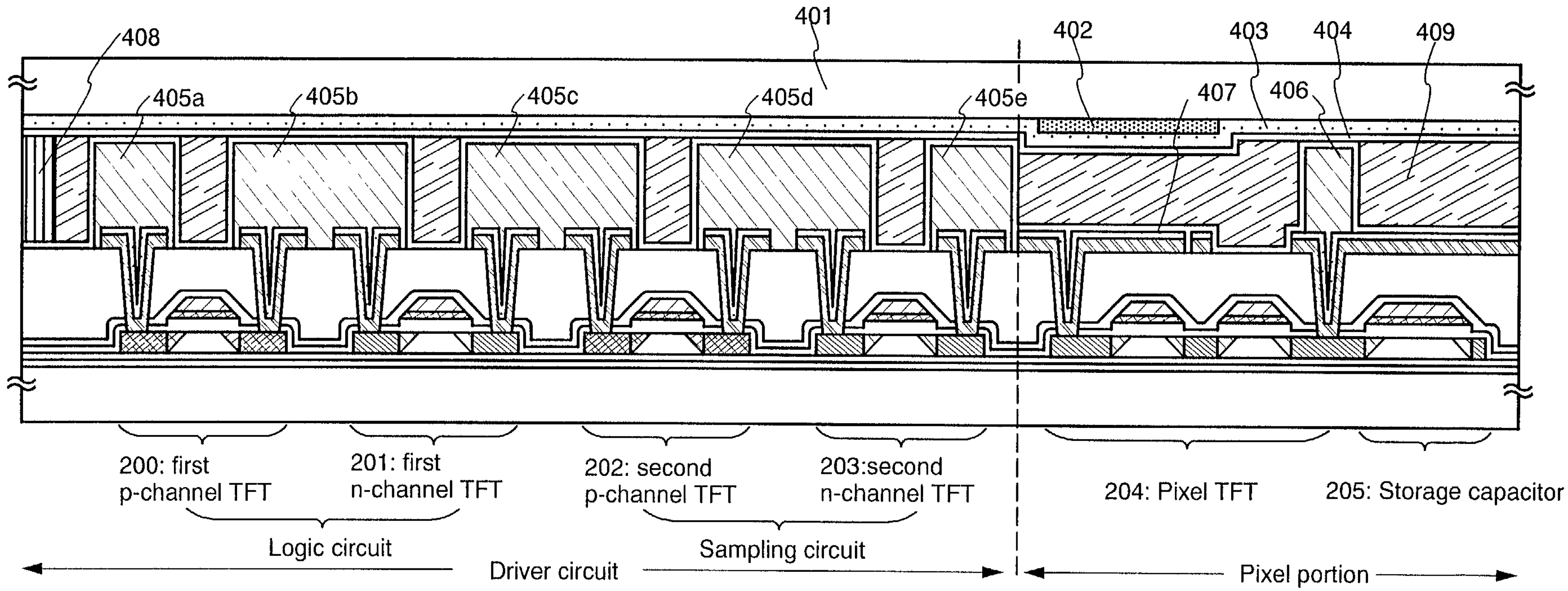


Fig. 14

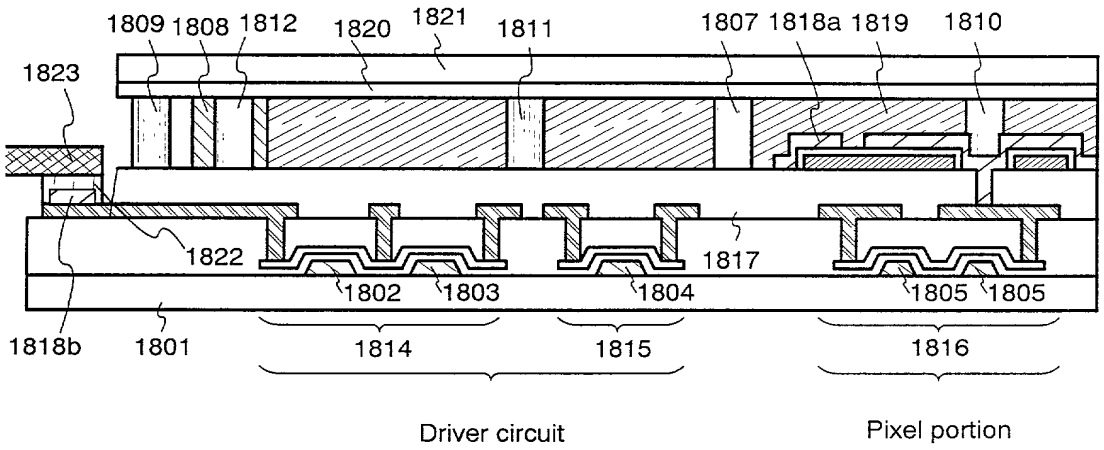

1809
1808
1812
1820
1821
1811
1807
1818a
1819
1810
1823
1822
1817
1802
1803
1804
1805
1805
1818b
1801
1814
1815
1816
Driver circuit
Pixel portion

Fig. 15A

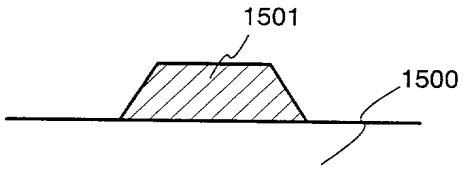


Fig. 15B

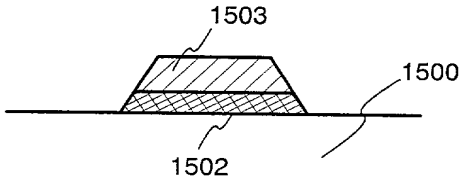


Fig. 15C

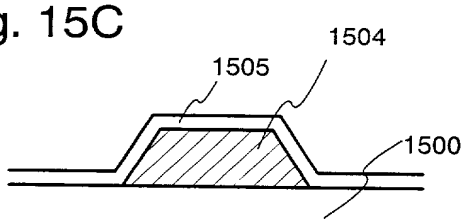


Fig. 15D

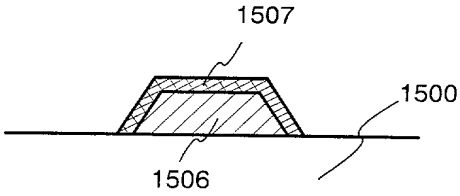


Fig. 15E

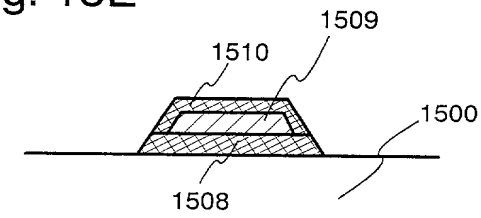


Fig. 15F

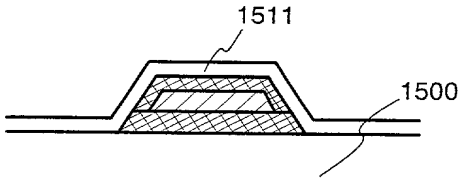


Fig. 16

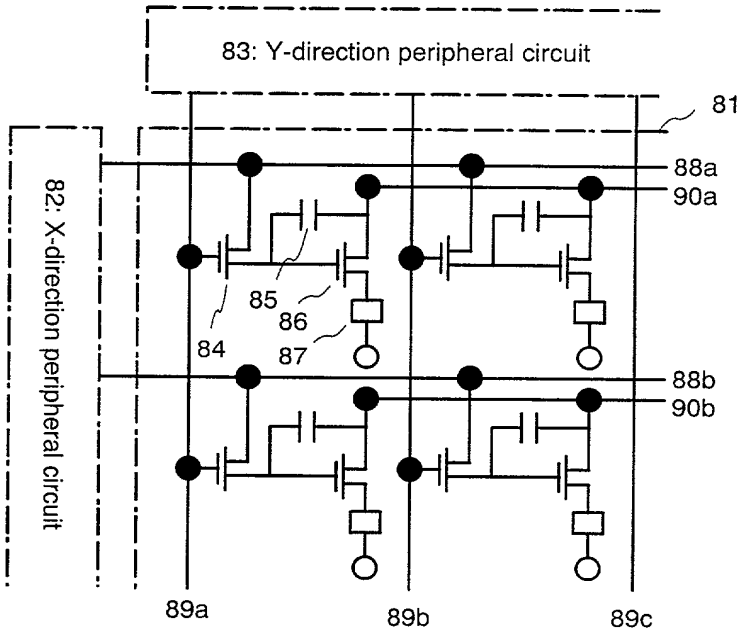
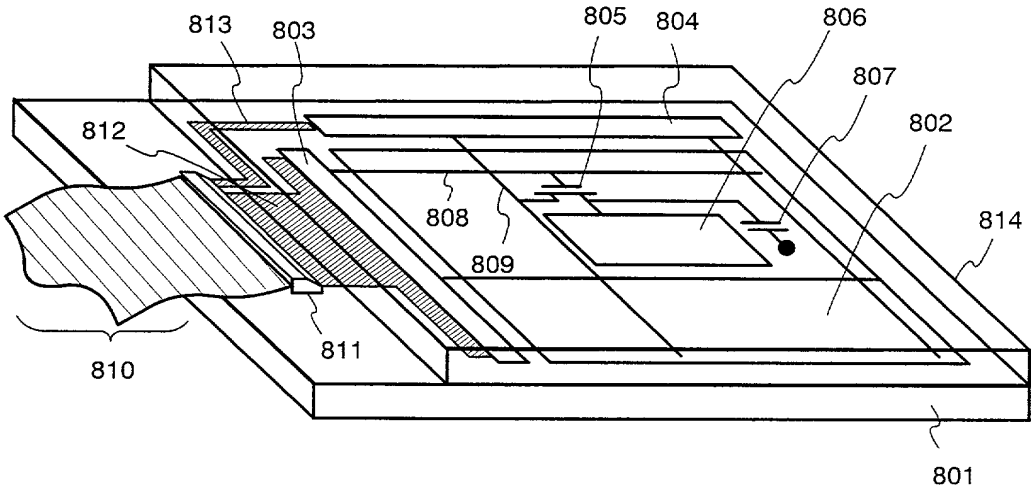

83: Y-direction peripheral circuit
81
82: X-direction peripheral circuit
88a
90a
85
86
84
87
88b
90b
89a
89b
89c

Fig. 17



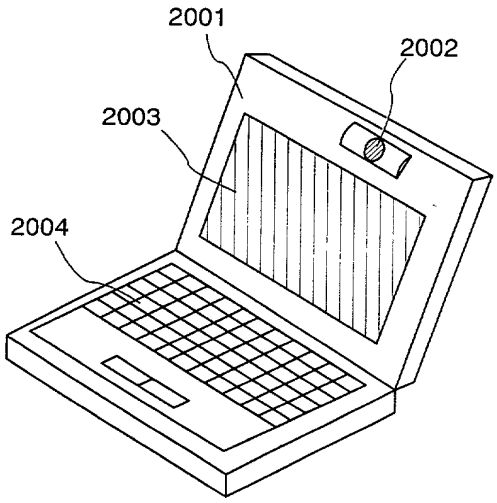


Fig. 18A

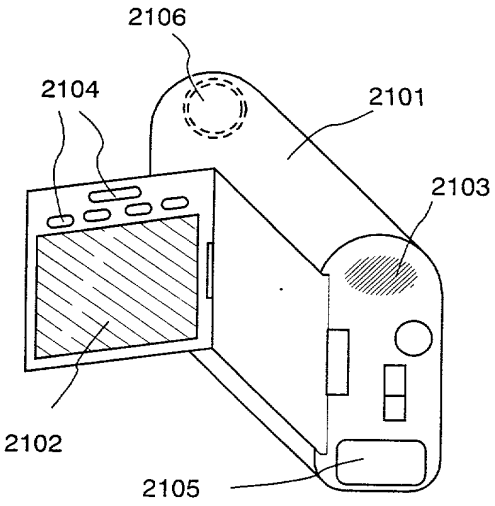


Fig. 18B

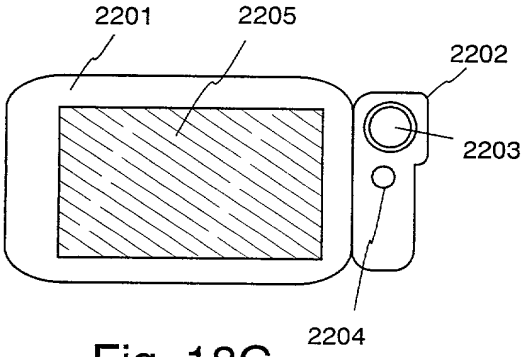


Fig. 18C

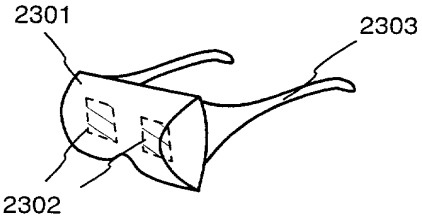


Fig. 18D

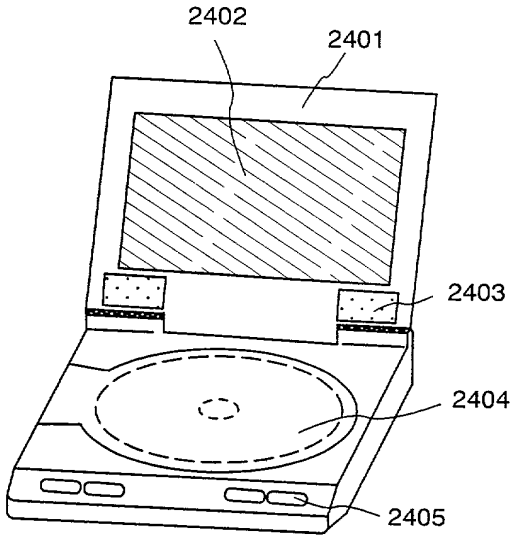


Fig. 18E

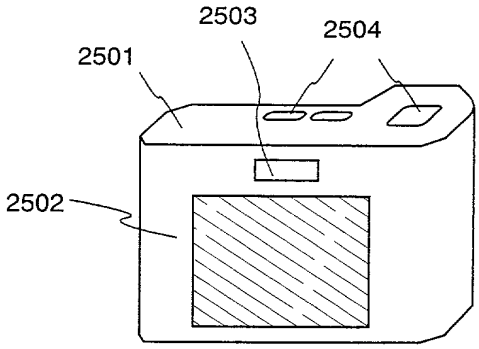


Fig. 18F

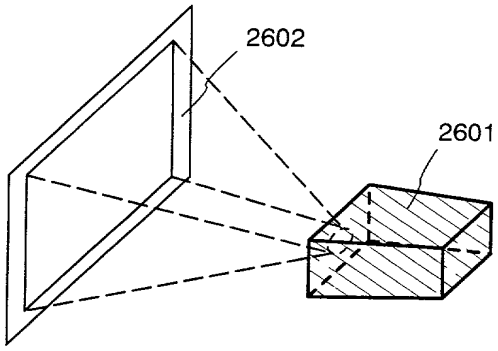


Fig. 19A

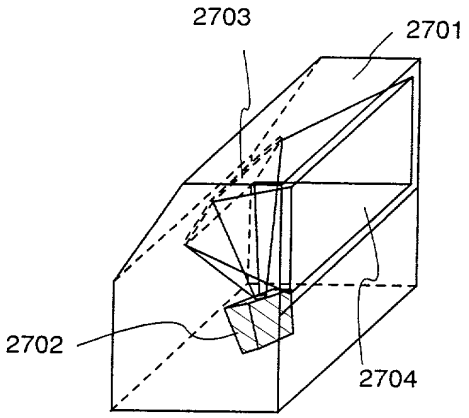


Fig. 19B

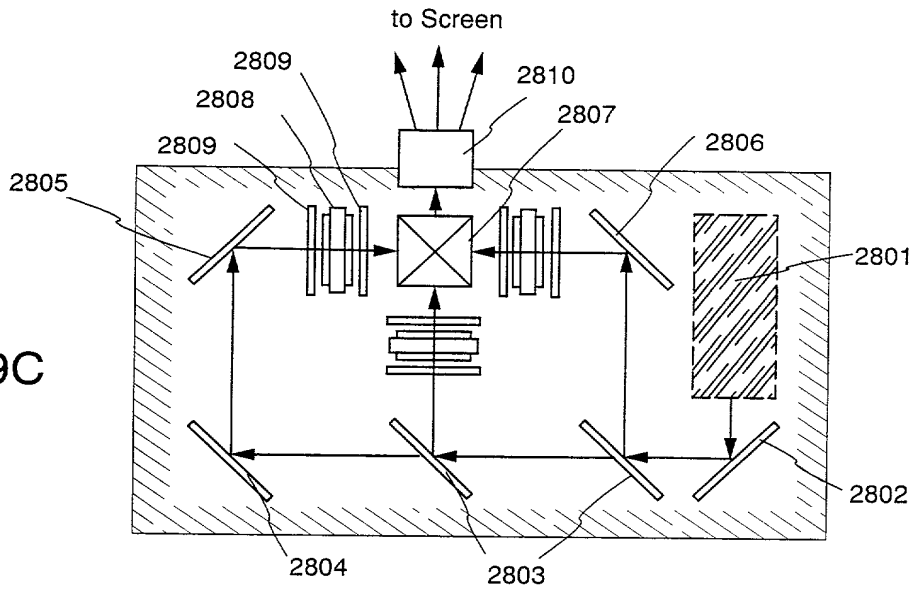


Fig. 19C

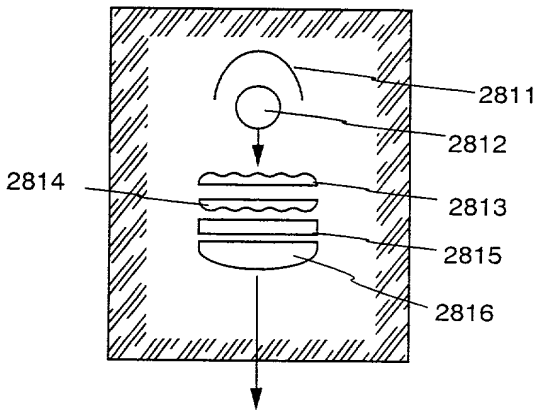


Fig. 19D

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration
日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者(下記の氏名が一つの場合)もしくは最初かつ共同発明者であると(下記の名称が複数の場合)信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

_____

_____

WIRING AND MANUFACTURING METHOD THEREOF, SEMICONDUCTOR DEVICE COMPRISING SAID WIRING, AND DRY ETCHING METHOD

上記発明の明細書(下記の欄で×印がついていない場合は、本書に添付)は、

The specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を__ __ __ __ __ __とし、(該当する場合) _____に訂正されました。

☐ was filed on _____as United States Application Number or PCT International Application Number _____and was amended on _____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第 35 編 119 条(a)-(d)項又は 365 条(b)項に基き下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約 365(a)項に基く国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

Priority Not Claimed
優先権主張なし

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	
11-206954	Japan	July 22, 1999	☐
			☐
			☐

私は、第35編米国法典119条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第 35 編 120 条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約 365 条(c)に基く権利をここに主張します。また、本出願の各請求範囲の内容が米国法典代 35 編 112 条第 1 項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規制法典第 37 編 1 条 56 項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

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(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況: 特許許可済、継続中、放棄済)

(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況：特許許可済、継続中、放棄済）
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状：私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁護士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number).

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